# Project X
Assessment Map

- 1. Portfolio
  - 1.1. Where does this product fit in your roadmap?
    - 1.1.1. Follow on to existing 2-chip solution (currently been designed-in with Bosch)
  - 1.2. What other things are interdependent with this product?
    - 1.2.1. Project X's main purpose is to qualify new process technology called SMTP9 (130nm logic + BCD-power devices)
  - 1.3. Where in the priority ranking does this product fit?
    - 1.3.1. Program is important as starting new platform for future window lift solutions
- 2. Market
  - 2.1. What is/are the target market segment(s) for this product?
    - 2.1.1. Automotive vendors
      - Door manufacturers (window lift system incl. mechanics) - i.e. Brose
      - Manufacturer of door subsystems (motor + electronics) - i.e. Bosch
      - Electronic subsystem (PCB in box) - i.e. Conti
    - 2.1.2. Considered quite homogenous market (commodity market), function for window lift is almost standardized
    - 2.1.3. Only segmentation could be "Einklemmschutz" yes/no & Diagnose request yes/no via LIN
  - 2.2. Have the segments been prioritized?
    - 2.2.1. Market is not considered segmented
  - 2.3. Who is/are the driving customers in the key segment(s)?
    - 2.3.1. Bosch
    - 2.3.2. Brose
    - 2.3.3. Conti
    - 2.3.4. And a few smaller ones
  - 2.4. What are the unique requirements for each segment?
    - 2.4.1. What is, if any, the impact of these on the product design?
      - Solutions are designed to work for above segments/applications
  - 2.5. How big is the market for this product?
    - 2.5.1. 60 Million parts per year in 2012
    - 2.5.2. Project X plans to capture 20% of this
- 3. Scope
  - 3.1. Project goal is to...
    - 3.1.1. Create window lift product which solves customer problem thereby selling 30 Million parts over 6 years. Qualified samples by end of 2010.
    - 3.1.2. Create chip which allows qualification of new vvvvv (combo of logic and power structures) processing technology. Technology release by May 2010 (T9).
    - 3.1.3. Create new product platform for follow on products also in other Product Lines
    - 3.1.4. Create "Showcase" to customers for new Process technology and SoC technology
    - 3.1.5. Create 6 Million Euro worth of re-usable circuit modules capable of being sold to other projects in the future
  - 3.2. At what stage are you now?
    - 3.2.1. Design implementation and verification of SoC IC
    - 3.2.2. Finishing and documenting the concept and the Internal Target Specification
  - 3.3. Why do this project?
    - 3.3.1. And why do it now?
  - 3.4. What is the project budget?
    - 3.4.1. 15 Million Euros (including 6 Million Euros for re-usable circuit macros)
  - 3.5. When is the target completion date?
    - 3.5.1. Target is "Qualified Samples" (QS) for mid 2010. Bosch is ok with this, but Brose feedback is that this is too late already.
    - 3.5.2. When asked, people (even some management) only know/care/think about tapeout
    - 3.5.3. Only a few people know ES, QS dates on top of their head
    - 3.5.4. Are you on schedule?
      - No. We are 6 months behind (with tape-out)
      - Tapeout (M6) was initially planned for July 2008, not clear whether we can do it before December 08 (no plan).
    - 3.5.5. What is your probability of achieving the target date on time?
      - Even a new target of 12/08 (for M6) is at risk.
    - 3.5.6. Initial Schedule (1st Silicon)
      - Idea Release (M1): 12/06
      - Feasibility Release (M2): 3/07
      - Project Release (=Kickoff) (M3): 9/07
      - Concept Release (M4): 3/08
      - Design Frontend Release (M5): 6/08
      - 1st (A11) Tapeout (M6): 7/08
      - 1st (A11) Silicon (M6.1): 12/08
      - 1st (A11) "Engineering Sample" Release to customer (M7): 4/09 (Communicated to customer)
    - 3.5.7. Initial Schedule (2nd Silicon)
      - 2nd (B11) Tapeout (M6): 6/09
      - 2nd (B11) Silicon (M6.1): 9/09
      - 2nd (B11) "Engineering Sample Release" to customer (M7): 11/09
      - Early Production Release "Production to Stock" (M8): 3/2010
      - "Qualified Samples" Delivery Release to customer (M9): 5/2010 (Communicated to customer)
      - Ramp Up Release (M10): 4/2011
      - Ramp up (M9): in 2010
- 4. Drivers
  - 4.1. Is time to market critical for this product?
    - 4.1.1. What is driving time-to-completion?
      - We are a year behind Freescale's competing SiP solution.
    - 4.1.2. What happens if you don't hit your target market entry window?
      - Bosch is contractually forced to by certain number of parts for certain price, otherwise they have to pay penalty. But even Bosch might opt out as a customer.
      - Brosi and Conti will not look at our solution
    - 4.1.3. What is the time window for maximum impact?
      - Need to have Qualified parts mid 2010, earlier is better
  - 4.2. Are you clear about what is needed to be delivered for the target completion time frame?
    - 4.2.1. Together with evaluation platform & FW/SW
      - Engineering Samples
      - Qualified Samples
  - 4.3. When is it too late (i.e. when should it be killed)?
    - 4.3.1. Difficult question due to the fact that Project X's main job is to qualify SMTP9 technology
    - 4.3.2. Killing Project X would also kill ccccc technology
      - True?
- 5. Success Criteria
  - 5.1. What are the criteria for evaluating success?
  - 5.2. What factors will be/are barriers to timely delivery?
    - 5.2.1. What are the top 3 technical problems or innovations needed?
      - Power control unit - Very low quiescent power
      - Successful integration of analog power circuits (ATOP) with digital micro-controller in new processing technology
    - 5.2.2. How would you overcome the barriers?
  - 5.3. What is the critical path?
    - 5.3.1. There is a macro plan (18 activities), but it's not clear how much it reflects reality.
    - 5.3.2. Completing and freezing the concept, completing the Internal target specification document
    - 5.3.3. Completing design implementation of chip
    - 5.3.4. Completing Functional Verification of chip
    - 5.3.5. Completing Layout and taping out chip
  - 5.4. How is the project organized (i.e. org structure)?
  - 5.5. What are the factors that currently promote/inhibit speed?
    - 5.5.1. Several key roles are not clearly defined and communicated (to team)
      - Chip lead
      - Concept Engineering lead
      - Overall engineering lead
    - 5.5.2. There is plenty of friction and frustration within the team
      - Team has many new people with various backgrounds and work styles and has never completed a project together
      - Team does a lot of rework since the handovers between people and teams are not well managed (lack of schdules)
      - "Team is held hostage by a diva" (Person X), who abuses his role and the rest of the team.
    - 5.5.3. Team seems to have a lack of internal resources and too many external contractors (also in key positions)
      - Need to be managed well
      - Need to be trained and brought up to speed, leave knowledge gap when they disengage
  - 5.6. What other "things" is this product/project dependent upon?
    - 5.6.1. Analog module development from VVVV design center
    - 5.6.2. Microcontroller sub-system development from MC business unit
    - 5.6.3. Support from MC for design-in and verification of MC SS
  - 5.7. Do we have the technology/IP required to develop this product?
    - 5.7.1. Process technology is developed/debugged while the chip development commences
      - Design package etc changes while team uses it
      - Models, P-Cells etc
    - 5.7.2. Team needs to set up and learn new design flow used for complex SoC chips (called Semi-Custom Highway)
    - 5.7.3. Team needs to learn how to use new tools and design flows (some are unproven, AMS models, P&R tool, bug-tracking tool etc.) while performing design
- 6. Cost of Delay
  - 6.1. Has cost of lateness been computed?
    - 6.1.1. What is the cost of delay (if known)?
      - ~20K Euro per day
    - 6.1.2. If so, is it believed and how is it used?
      - Believed by the PGM, not used by the team
    - 6.1.3. Does it create urgency?
      - It does not look like it. The team clearly has other issues to deal with.
- 7. Customer
  - 7.1. Who is/are your customer(s)?
    - 7.1.1. Current Customers
      - Bosch
        - Manufacturer of door subsystems (motor + electronics)
        - Talk to Bosch every 4 weeks (PGM & Apps) - currently in process of going through Target Specification with Bosch (to validate it)
        - In process of designing-in the Project X predecessor solution (2-chip solution)
        - IFX AP has a good relationship with Bosch, and think it's likely to get them to sign up for Project X
    - 7.1.2. Additional desired Customers
      - Brose
        - Door manufacturer (window lift system incl. mechanics)
        - Talk to Brose every 3 months
        - IFX AP has no market share with Brose
        - Is using Freescale 2-chip solution
        - Interested to look at Project X when available, but will only change if good reason (price) available.
      - Conti
        - Electronic subsystem (PCB in box)
        - Talk to Conti every 6 months
        - Same as Brose
  - 7.2. What customer problem is the product going to solve?
    - 7.2.1. How is your product doing this better than your competition?
      - Competition
        - Project X is currently NOT solving the customer problem better than the competition
        - Freescale micro controller is common in industry, while IFX uC is not common (=possible barrier to entry)
        - The only possible differentiation is with ASP/price, but currently Project X ASP is at boundary of what customer's are willing to pay (90 cents in 2010/2011)
        - Freescale (the #1 competitor) - with having a good 2-chip solution and a single-placement (2-die) SiP solution. Considered one year ahead.
        - Elmos (smaller German company) - 2 chip solution
  - 7.3. What do your customers value?
    - 7.3.1. What do the customers want from the product (top 5 reqs)?
      - Lowest Price/ASP (especially Brose, Conti)
        - Scalability in terms of price (i.e. take out unneeded memory to cut price)
      - Flexible power management -Very low quiescent power & low on-power
      - Window Lift system "Standard" Feature set
        - dddddd
      - Platform concept
        - Stay with one vendor
          - True for Bosch, not for Brose, Conti
        - Resistance to change uC development platform (SW development)
      - Ease of developing window lift solution (SW, HW) with the chip
        - Good Support
        - Good development tools (Eval board, GUI, SW environment)
      - Solution size (footprint) is not (?) important
        - Different people tell different things here...
    - 7.3.2. Where is the product to be deployed or sold?
      - Worldwide
        - US will mandate a law that every window (not just driver side) needs dddddd
- 8. Requirements
  - 8.1. Do you know what is needed, and when?
    - 8.1.1. Looks like they have an ok idea
  - 8.2. What other "things" must accompany the product for it to be successful (other products, etc)?
    - 8.2.1. Need to reduce production (ATE) test time by wafer-testing 32 parts in parallel (to hit COGS target)
  - 8.3. Do you use a formal process for voice of the customer & aligning customer needs with project requirements?
    - 8.3.1. This project has NO (!) Marketing requirements document (MRD)
    - 8.3.2. They went straight to creating the Target Specification (customer facing) and then Internal Target Specification (development team facing)
  - 8.4. How do you identify project requirements?
    - 7
  - 8.5. How will you manage changing requirements?
    - 8.5.1. Change request process into Target Specification
  - 8.6. How will you cope with uncertainty in requirements?
    - 8.6.1. Plan is to get an understanding of the customers problem/application and anticipate his needs that way.
- 9. Schedule
  - 9.1. Does the team have/utilize a well defined program schedule?
    - 9.1.1. Absolutely no.
    - 9.1.2. They use >8 schedules for various purposes in various formats (Excel, MSP) and "styles"
      - Process technology schedule is Powerpoint slide
    - 9.1.3. Most of these plans are not updated with actuals and are outdated (stale)
    - 9.1.4. Schedules do not define ownership for deliverables and milestones
  - 9.2. Do you know the gap between target delivery and actual date?
    - 9.2.1. No. Currently they have no clear visibility when their next major milestone (tape-out) is going to happen. Expect it to be November/December 2008 ("gut feeling")
  - 9.3. Do you meet with the team to update your schedule one or more time per week with actual data and then attempt to pull-in to close the gap?
    - 9.3.1. Have started recently to try doing this.
  - 9.4. Was the complete team involved in developing the schedule?
    - 9.4.1. Is the team bought in (do they believe the schedule is realistic)?
      - Team does not trust the plans and dates
    - 9.4.2. Did you start planning using a macro plan? How did you do it?
      - Started with an Excel based macro plan
      - Created it and then showed it to team
  - 9.5. Has the full team been involved in exploring alternative ways of accelerating the schedule?
    - 9.5.1. No
  - 9.6. Is there a contiguous critical path from start to end in your schedule?
    - 9.6.1. No. It's distributed over several un-connected plans.
  - 9.7. Is the schedule used to drive the work in the project?
    - 2
  - 9.8. Do you use the schedule to manage milestone trends?
    - 9.8.1. No milestone trends are created
  - 9.9. Do you know what your critical path is?
    - 9.9.1. Not really
    - 9.9.2. There is a macro plan which kind of shows "some" CP, but it's not updated regularly and broken down enough in near term to drive the work
  - 9.10. Are resources overused or pulled in and out of the project by other work?
    - 9.10.1. Key resources are totally overloaded by performing several Project X functions in parallel.
    - 9.10.2. The project has been started with insufficient resources. To keep going they hired an "Army" of contractors.
    - 9.10.3. The program seems to have ~40% external contractors (~20 people)
  - 9.11. Is the team organized around the major customer deliverables? (rather then functional)
    - 9.11.1. No, it's organized functional.