Weekly schedule refresh

Weekly program status • 22 April 2026

1. Status summary

First significant pull-in of the program — 23 days on the qualification milestone. The new quality lead completed a detailed replan of the qualification phase, cutting execution from six months to four months (240d → 150d) and qualification report writing from 60 days to 30 days. In parallel, a **shared-risk qualification path** at 168-hour HTOL has been added to enable the lead customer to start application qualification in parallel with full product qualification. Net effect: WS: Product qualified predicted pulls in from 30-Apr-28 to 7-Apr-28, closing the gap to target from 152 to 129 days. WS: Samples available shows no change this week — still predicted 3-Sep-27 (65-day gap). FS wafers have not been re-baselined yet despite the foundry partner running ahead; the program manager plans to break down the 117-day foundry task into process stages over the coming weeks and expects a further 1–2 week pull-in once the data is ingested.

Milestone	Target	Predicted	Gap	Change
WS: Samples available	30-Jun-27	3-Sep-27	**(65)**	**No change**
Product qualified	30-Nov-27	7-Apr-28	**(129)**	**+ 23 days (pull-in)**

Key wins this week: Foundry-partner management meeting held — four company attendees including the program manager had a productive, candid exchange; the foundry confirmed the 3-day/mask-layer assumption, shared their internal dZ waterfall chart, and set up a bi-weekly cadence. Actual wafer progress is tracking slightly ahead of the foundry's own schedule. **Second critical path** (TC1 wafer starts) was pulled in 11 days on the back of the foundry's confirmation — now at 35 days from CP (was 24 days). OSAT-partner tester/prober spec progress continues but the sourcing lead encountered a commercial-terms snag on the term sheet; he is splitting engineering and commercial tracks to unblock engineering access immediately. **Customer engagement escalated** — the customer contact responded, meeting with the customer COO secured for April 28; the test engineering lead is finalising functional test spec this week with a customer-ready version next week. The new quality lead has formally taken ownership of all qualification tasks (Task 324+), closing the handover action from last week.

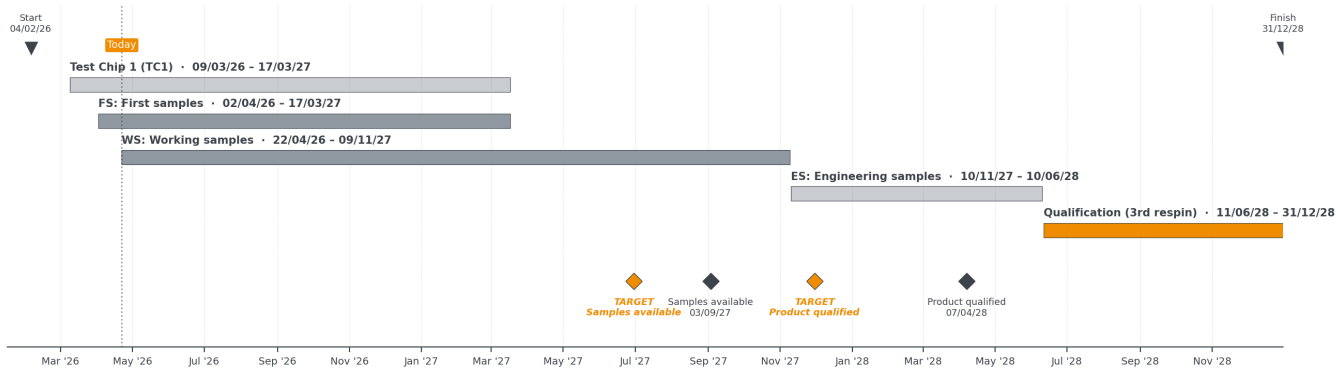


Figure 1: Program timeline

2. Schedule and trends

Critical path. The critical path is structurally unchanged through to WS samples but the tail has been compressed. Sequence: FS: Wafer starts to ALD-DEP (117d, process lead, 0 float) → ALD vendor processing (30d) → Reinsertion (63d) → First-silicon wafers out (11-Nov-26) → Validate sort (30d, validation engineer) → Ship & assemble (7d) → Final test (30d) → Samples available (17-Jan-27) → Validate design (package, 45d, design lead) → WS redesign (30d) → Final masks → WS samples available (3-Sep-27). Downstream, the **qualification tail has been shortened**: Execute Qualification now 150d (was 240d), Complete Qual report now 30d (was 60d), Qualification Done now 7-Apr-28 (was 30-Apr-28). The phase has also been renamed *Qualification (3rd respin)* to reflect the planning basis. Critical attention remains on the 117-day foundry fab window and the August 10 ALD-DEP hold date; decomposition of the foundry task into FEOL / gate / contact / metal stages is the next schedule improvement.

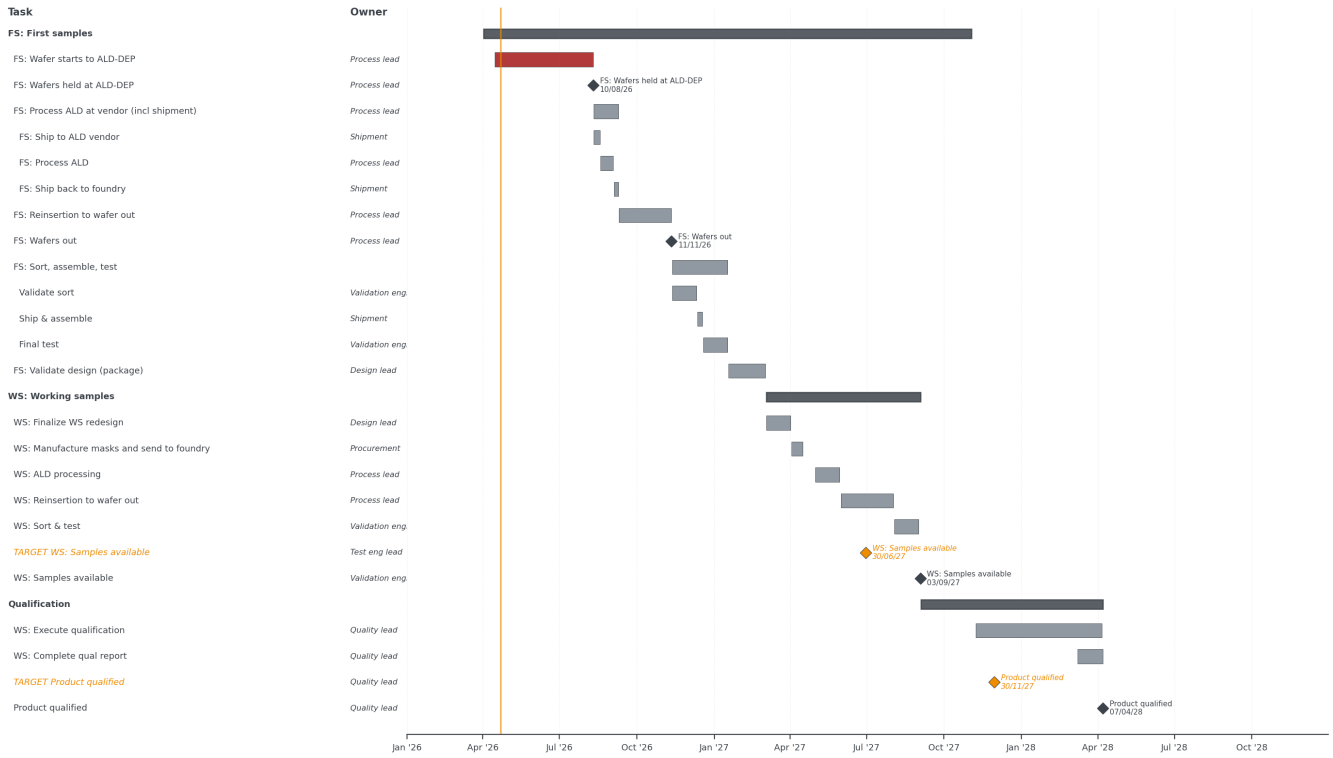
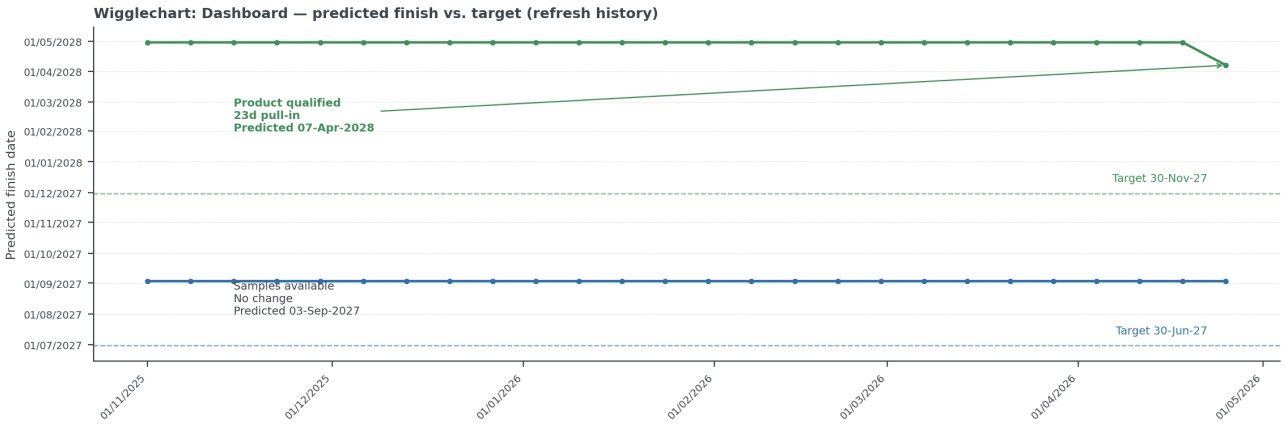


Figure 2: Critical path (extracted from program schedule)

Wiggle chart. The qualification milestone shows the **first material pull-in since tracking began** — predicted finish moves from 30-Apr-28 to 7-Apr-28 (+23 days, green trend arrow). The risk indicator on qualification has flipped to pull-in. WS: Samples available shows zero change this week: trend holds at 3-Sep-27 with the 65-day gap intact, because the FS critical chain has not been re-based against the latest foundry data yet. Cause of change recorded: *"Pull-in due to reassessing qualification timelines with new quality lead."* This is a directionally positive week but the structural 65-day gap on WS samples remains the governing constraint.



Target milestone	Target date	Predicted finish	Schedule gap	Risk	Change since last	Trend	Cause of change	Actions
Samples available	30-Jun-27	3-Sep-27	(65)		0	→	No change	Discuss mitigation options for ALD deposition. Owner: Validation eng. Due: 3-Apr
Product qualified	30-Nov-27	7-Apr-28	(129)		+23	↗	Pull-in due to qualification timeline reassessment.	—

Figure 3: Wigglechart dashboard (extracted from refresh tracker)

Critical path analysis. Significant reshuffling of the near-critical paths this week. **CP2 and CP3 have swapped**: last week's CP2 (TC1: Wafer starts to ALD-DEP, process lead) was pulled in 11 days on the back of foundry confirmation and is now CP3 at 35 days from CP. The new CP2 (31 days from CP) is a test-hardware-lead / COO cluster: Sort 1 tester/prober spec from the OSAT partner (2d), Sort 1 probe-card design (14d), and FS procurement approval for package testing infrastructure (7d, COO). CP4 (37 days from CP) shifted by 90 days due to a newly-discovered package-test-spec dependency but retained its margin; it now runs through the test engineering lead's Sort 1 functional test spec (46d) and the offshore package test lead's package-test-fixture design (45d). The team agreed to continue monitoring CP2 through CP4 weekly and to watch whether the test-hardware-led cluster creeps closer to zero float as probe-card design kicks off.

Other schedule updates

- **Qualification phase replanned by quality lead.** Execute Qualification compressed from 240d to 150d (6 months → 4 months); Complete Qual report from 60d to 30d. Qualification start now gated on Design validated rather than Samples available, which the team flagged as the technically correct dependency. Phase renamed *Qualification (3rd respin)*.
- **Shared-risk qualification path added** at 168-hour HTOL (vs. standard 1000-hour), enabling the lead customer to begin application qualification in parallel with product qualification — saves the customer approximately 2 months. Activation-energy and acceleration-factor calculations to be confirmed by the quality lead.
- **Foundry management meeting held.** Open communication with the foundry partner, bi-weekly cadence set, foundry confirmed 3-day/mask-layer commitment, foundry shared their internal dZ waterfall chart. Company tracking aligned with foundry tracking. The process lead is updating the mask-level crawl chart 3× per week and will share via meeting minutes.
- **OSAT term sheet — commercial snag.** The OSAT partner wants commercial terms agreed before releasing technical contacts. The sourcing lead is restructuring into two parallel tracks: engineering pricing agreement first (to unblock engineering access), commercial / production terms in parallel. Estimate remains ~2 weeks. Successor linkage of OSAT tasks to the signed term sheet still outstanding — action assigned to the program manager.
- **ALD vendor engagement meeting** scheduled for May 5 to align on ALD demo window. Original vendor readiness was 23-Jul which is earlier than wafer arrival; current discussions exploring combined FS+TC1 ALD shipment. Vendor lab is not high-volume and protocol maturity will be checked on-site; live demo required.
- **Customer engagement escalating.** Meeting secured with the customer COO on April 28. The customer requires “organisational maturity” evidence — product spec, detailed test spec, and qualification spec. The test engineering lead is finalising functional test spec this week; customer-condensed version to follow next week. Customer milestones not yet carried in the schedule — deliberate, pending customer-engagement maturity.
- **Design validation plan debate.** The customer engagement lead and the sourcing lead raised that the 45-day design validation block has no formal plan document, making duration a low-confidence estimate. The test engineering lead confirmed a bring-up / validation test list exists but is not formalised as a plan. Action: test engineering lead to align with the design lead and share; team to decide next week whether a formal validation plan task is added.
- **Package test spec dependency added.** New predecessor chain identified in-session — the offshore package test lead's package-test-fixture design feeds the package test spec, which feeds the test hardware lead's package test program development. Critical path 4 absorbed the shift without losing float.
- **Foundry actual wafers ahead of schedule.** Actual wafer progress (per foundry's dZ waterfall) is slightly ahead of their own schedule at early mask levels. Cautious optimism — 3-day/mask tracking established as the crawl-chart baseline.
- **Second lot tracking.** The foundry's second lot (staggered by two weeks) continues; primary schedule tracks lot 1 only; team tracking both separately.

3. This week's tasks

The **process lead**'s FS: Wafer starts to ALD-DEP (CP 1, 0 days float, 117 days) remains the program driver — the foundry lot is running and mask-level tracking is now in place. The **test hardware lead** now owns the new CP 2 cluster (31 days from CP): obtain OSAT tester and prober spec (2d, overdue), issue Sort 1 probe-card PO (quote in hand from the test-card vendor), then design Sort 1 probe card (14d). The **COO**'s FS procurement approval for package testing infrastructure (7d) sits on CP 2 and must precede the package-test-fixture PO with its 150-day lead. TC1: Wafer starts to ALD-DEP (**process lead**, CP 3, 35 days from CP, 125d duration) is the second wafer path to watch. The **test engineering lead** is driving Sort 1 functional test spec (CP 4, 46d, 37 days from CP) — target finish 24-Apr — and will then produce customer versions for the lead customer. The **offshore package test lead** owns package-test-fixture design (CP 4, 45d). The **tool vendor liaison** has TC1: Secure agreement with the ALD vendor (CP 10, 5d) — this is the procurement gate for the TC1 ALD slot. The **sourcing lead** is running OSAT term-sheet negotiation (CP 9, 22d) with restructured engineering-first approach. The **validation engineer** hit SPI2: Sort 1 (CP 8, 9d) this week.

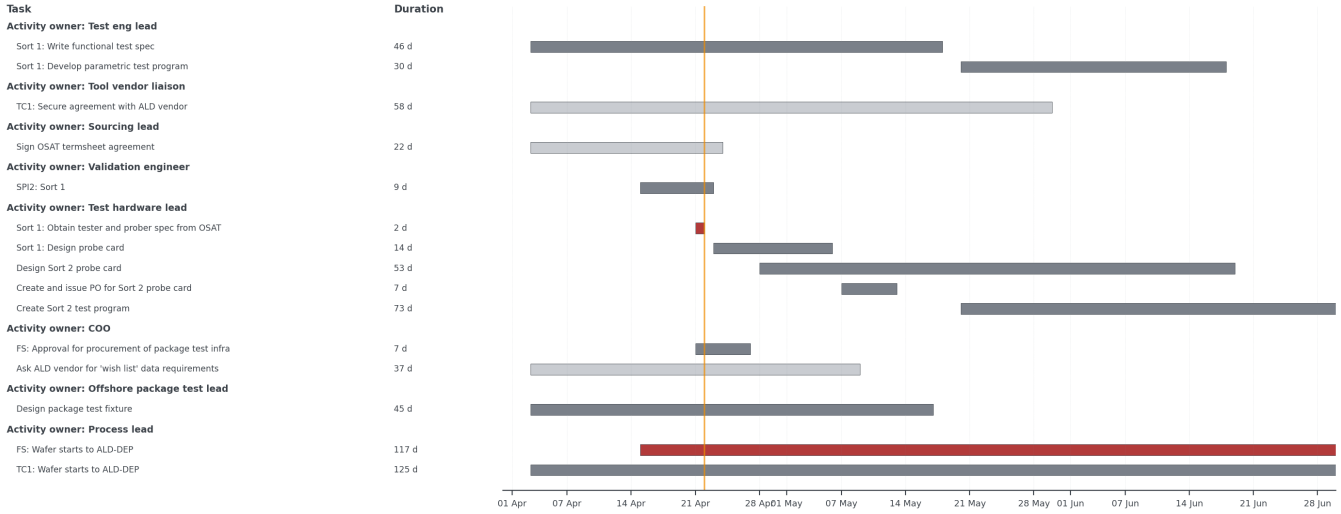


Figure 4: Focus report — work by owner (extracted from program schedule)

4. Actions

Prior actions closed: Transfer qualification tasks (Task 340+) to the new quality lead (program manager / test engineering lead / quality lead, due Apr-26) — closed: quality lead now owns all qualification tasks in the schedule and has replanned the phase. Break down the foundry's 117-day fab task and prepare for the April 27 foundry management meeting (program manager / process lead, due 27-Apr) — meeting held, closed; follow-up decomposition into FEOL / gate / contact / metal stages rolled into the open “Confirm foundry estimate” action. Set up foundry lot-tracking (process lead, due Apr-26) — closed: bi-weekly cadence and 3×/week crawl-chart tracking now established.

New / open actions:

#	Owner	Action	Due	Source
1	**Validation engineer**	Discuss mitigation options for ALD deposition (WS: Samples available). Carried over multiple weeks — needs resolution or formal closure.	**3-Apr-26 OVERDUE**	*Action log*
2	**COO**	Push the foundry to process faster — management meeting held; continue pressure on lot prioritisation through new bi-weekly cadence.	27-Apr-26	*Action log*
3	**Program manager**	Follow up with the sourcing lead on signing the OSAT termsheet agreement to assign successor links in the schedule (signed term sheet is a predecessor to multiple OSAT tasks).	29-Apr-26	*Action log*
4	**Program manager**	Confirm foundry estimate of earlier delivery for FS: Wafer starts to ALD-DEP. Ingest mask-level data and break the 117-day task into FEOL / gate / contact / metal stages.	5-Jun-26	*Action log*
5	**Process lead**	Align with the foundry liaison on argumentation for the foundry to shorten Reinsertion time (FS: Reinsertion to wafer out) — leverage the sourcing lead's ALD contamination-protocol data.	5-Jun-26	*Action log*
6	**Sourcing lead**	Execute split OSAT strategy — send engineering pricing list, get OSAT to release engineers immediately, pursue commercial / production agreement in parallel. Target completion ~2 weeks.	6-May-26	*Schedule*
7	**Test engineering lead**	Complete Sort 1 functional test spec (target 24-Apr) and produce customer-ready condensed version (aim for next week). Have the sourcing lead sanitise before sending.	1-May-26	*Schedule*
8	**Test engineering lead**	Plan out all test specification milestones (parametric, functional, package test, qualification spec) and share with the COO so dates can be communicated to the customer.	29-Apr-26	*Schedule*
9	**Test eng lead / Design lead**	Align on and share design validation plan / bring-up test list. Team to decide next week whether a formal validation plan task should be added to the schedule.	29-Apr-26	*Schedule*
10	**Quality lead**	Confirm activation-energy and acceleration-factor calculations for the 168-hour shared-risk HTOL qualification path; document customer-facing assumptions.	6-May-26	*Schedule*
11	**Test hardware lead**	Obtain tester and prober spec from the OSAT partner (overdue). Issue probe card design PO upon receipt of spec (quote in hand from the test-card vendor). Kick off Sort 1 probe-card design (14d).	29-Apr-26	*Schedule*
12	**Test hardware lead / COO**	Secure COO procurement approval (7d) for package testing infrastructure (150-day lead). Place PO immediately after approval. Maintain OSAT test-time rental as fallback.	15-May-26	*Schedule*
13	**Process lead**	ALD vendor meeting 5-May — prepare for ALD demo alignment; push the vendor for cut-off date on TC1 ALD window re-slotting; evaluate combined FS+TC1 ALD shipment option.	5-May-26	*Schedule*
14	**Process lead / Program manager**	Decide on alternative ALD partner vs. primary vendor lab. Meeting deferred from previous Friday.	25-Apr-26	*Schedule*
15	**Test engineering lead**	Align with offshore package test lead on package-test-fixture spec and test-program development — these activities need to start now given long lead times.	29-Apr-26	*Schedule*
16	**Program manager**	Propose an async update mechanism for the offshore package test lead given timezone conflict with the weekly refresh meeting. Ensure their input is captured weekly.	29-Apr-26	*Schedule*
17	**COO / Customer engagement lead**	Following April 28 customer COO meeting, determine when customer milestones can be formally added to the schedule (currently held out).	8-May-26	*Schedule*

5. Risks

Risk	Description	Severity
Structural schedule gap	WS: Samples target 30-Jun-27 vs. predicted 3-Sep-27 — 65-day gap **(unchanged this week)**. Product qualified target 30-Nov-27 vs. predicted 7-Apr-28 — 129-day gap (**improved by 23 days** via the quality lead's qualification replan and 168h HTOL shared-risk path). Structural gap on WS samples remains the governing constraint — further foundry-task decomposition expected to yield 1–2 weeks more, but closing the 65-day gap still requires replan or parallelism change.	*Critical*
Foundry fab cycle time	Now materialising but **trending better**. FS lot running since April 15; foundry's actual wafer progress tracking slightly ahead of their own schedule at early mask levels; 3-day/mask commitment confirmed; dZ waterfall visibility gained; crawl-chart tracking 3×/week. Bi-weekly cadence established. Remaining concerns: 117d is still a single monolithic task pending decomposition; reinsertion 63d and PM windows remain uncertain; FS wafers have not been re-based against newer foundry data yet.	*Critical*
Test hardware lead times	Unchanged this week. Probe-card PCB 70d (was 42d); Package test infrastructure 150-day lead time; approval + PO + lead = ~167 days. Vendor still unresponsive. Probe-card PO unblocked by quote in hand but design gated on OSAT tester/prober spec. OSAT test-time rental remains fallback but cannot support design validation at speed.	*Critical*
OSAT dependency chain	Worsened slightly — the OSAT partner pushed back on releasing engineers before commercial terms agreed. The sourcing lead has restructured into parallel engineering + commercial tracks to unblock tester/prober spec delivery. NDA signed; PO quote in hand; tester/prober spec still pending. Successor linkage of OSAT tasks to the signed term sheet still outstanding (program manager follow-up).	*Critical*
Owner concentration	The process lead now owns CP1 (FS lot, 0d) and CP3 (TC1 wafer starts, 35d). The test hardware lead owns the new CP2 cluster (Sort 1 tester spec, probe card) and CP6 (Sort 2 tester). Load on these two individuals is a systemic risk — any absence or competing priority hits multiple paths. No deputy or backup author assigned yet for the most critical individual tasks.	*High*
Design validation scope	**New this week.** 45-day design validation block has no formal validation plan document; the customer engagement lead and the sourcing lead flagged this as a low-confidence duration and open-ended activity. The test engineering lead confirmed an informal bring-up / validation test list exists. Risk: validation drifts open-loop once started, amplifying downstream WS and qualification variance. Test eng lead and design lead to align and share; formal task TBD next week.	*High*
Customer alignment / spec readiness	**New this week.** April 28 meeting with the customer COO raises customer commitment; the customer requires product spec, detailed test spec, and qualification spec as evidence of organisational maturity. The test engineering lead is completing functional test spec this week; customer-ready condensed versions to follow. Current schedule does not carry customer milestones — could cause surprises as the customer's own qualification planning firms up.	*High*
Foundry escalation approach	Materialised and trending positive. CEO / management meeting held; bi-weekly cadence set; relationship preserved. Continuing risk: if wafer progress stalls, the escalation lever is now partially spent. Maintaining face with foundry management remains culturally important.	*High*
ALD vendor capacity & ALD window	ALD vendor meeting May 5. Original demo readiness 23-Jul is earlier than wafer arrival; combined FS+TC1 ALD shipment under discussion. Vendor lab is not high-volume; contamination-protocol maturity unverified; live demo and protocol audit required. Reinsertion contamination concerns (historical nickel data) add pressure.	*High*
Near-critical paths reshuffling	CP2/CP3 swapped this week. CP4 absorbed a 90-day shift without losing float. Schedule is still plastic and sensitive to small duration changes. Need to watch whether the test-hardware-led CP2 cluster closes on zero float as probe-card design kicks off.	*Medium*
Procurement gaps	Substantial progress on procurement breakdown completed over last two weeks. Remaining: cash-flow forecasting, backup OSAT qualification, and location-tagging of all schedule tasks (program manager).	*Medium*
BIST design issue	Potential built-in self-test problem flagged previously by the COO and sourcing lead. Still under investigation; no schedule impact yet.	*Medium*
Offshore communication	Time-zone conflict — early hours offshore for the weekly refresh meeting. No update received in the report this week. Tuesday sync with the test hardware lead continues but async mechanism needs improvement. Substrate design has not yet started despite NDA being signed.	*Medium*