A lateralworks case study in decision by silence

The thread that read as agreement

November 2026 · lateralworks · Source: a client email thread, names and identifiers removed [1]

Nobody in this thread disagrees with the plan. They disagree about which wafers ship and what package gets built, and it is written so politely that headquarters will read it as agreement. The Taiwan director ships two wafers tomorrow unless someone objects by the end of his day. The Japan test director may have objected.

What each message says

Who	What they wrote	What it means
Design lead (HQ), via the program lead	Silicon validation findings make it critically urgent to check the memory interface at full speed; blind assembly and package testing	"Validation found a problem. We need packaged parts fast to see if the interface runs at speed. Four interface tests, no memory array. Single-die is enough; DDP only if the assembler is faster that way."
Taiwan director, first reply	[The assembly lead] is the key player who works with [the assembler] closely… I would help him if needed	"The assembly lead owns the assembler, not me. I will support."
Japan assembly lead	I need wafer information (Parts No, Lot No) to issue PO to [the assembler]	"I am blocked. Give me the lot and part numbers and I will raise the PO."
Taiwan director, second reply	We will send those 2 [product] wafers. Pls raise it if any objection by end of today, then I will start shipping tomorrow	"Here are the two wafers. Silence by the end of my day means I ship tomorrow."
Japan test director	We'd like to make a clear the wafer shipment… three wafers with full patter… other two wafers for CP program debugging… two wafer shipment means DDP package… takes a long time… consider an SDP package… we rely on [headquarters]'s decision	"Wait. Which two wafers? Japan needs two of the three for CP program debug (CP is chip probe, the wafer-level test). Two wafers means dual-die; that setup is slow. If urgent, build single-die. Headquarters decides; we will not."

Three decisions nobody is holding

1. **Package.** The design lead says single-die (SDP) is sufficient, and dual-die (DDP) only if the assembler is faster. Japan says DDP setup takes a long time. By the design lead's own rule that settles it: SDP. Nobody has written it down.
2. **Wafers.** The thread names "3 setup wafers", "2 product wafers" and "three wafers with full pattern" and never says which are which, or whether assembly consumes Japan's CP debug wafers.
3. **Owner.** The program lead gave the Taiwan director the lead, who handed the assembler to the assembly lead. Japan waits on headquarters. The package decision has no owner.

First move. The design lead sends one reply today, program lead on copy, before the Taiwan day ends: SDP; these two wafers by lot number; Japan confirms CP debug is unaffected; the assembly lead names what the PO still needs. Reply by email, not by silence. Draft in Appendix C.

The plan is not at risk. The reading of it is. Three languages need a native speaker at each end.

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Appendix A

The plan, as written

Silicon validation found something that makes one question urgent: does the memory interface run at its target speed? The full test flow cannot answer that quickly, so the plan is to build packaged parts blind, before wafer-level test has proven the die, and run four narrow interface tests that need no memory array. The stretch goal is to get the answer in time to put metal fixes into further silicon [1]. Dates are shown as weeks from the plan's first due date.

Plan and due dates

#	Workstream	Action	Owner / support	Due
1	Blind assembly	Select 2 of the 3 setup wafers as pipeline cleaners; submit the assembly request to the assembler's subcontractor; move 2 product wafers from the foundry	Assembly lead / Taiwan director	Week 1 Thu
2	Blind assembly	Mechanical trial on setup wafers (< 1 week) — results	Assembly lead / Taiwan director	Week 2 Mon
3	Blind assembly	Submit and start the assembly request for 2 product wafers	Assembly lead / Taiwan director	Week 2 Tue
4	Test program	Simulation test cases + design documentation for the 4 debug tests (2 working days per item)	Design (HQ) — design manager to assign	Week 1 Thu → Week 2 Fri
5	Test program	Test code, cascading from each simulation test case	Japan test engineer	Week 4 Tue
6	Test program	Early test program debugged	Japan test engineer	Week 5 Wed
7	Testing at the assembler	Test fixture board with mounted packages — request to the assembler	Japan test director / advisor, Taiwan director	Week 5 Tue
8	Testing at the assembler	Sanity check on the fixture (program load, continuity, power-up)	Japan test director / advisor, Taiwan director	Week 5 Thu–Fri
9	Testing at the assembler	Start testing on the rented tester	Japan test engineer	Week 6 Mon
10	Testing at the assembler	Test report	Japan test engineer	Week 7 Mon

Package, in the design lead's words: a single-die package (upper die position left empty) is sufficient for these tests. If the standard DDP route is faster at the assembler, go ahead with the default DDP; the test program covers both [1].

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The four early tests

#	Test	What it tells us	Test case due
1	Clock and strobe test	No read or write command at all, so immune to both known interface bugs. Checks clock in, strobe in, data out at speed	Week 1 Thu
2	Fixed-pattern read at speed	The key test for “does the strobe come back on a read”: no array, no write, known data	Week 2 Mon
3	Write → read loopback without the array	Full write and read data path at speed. Separates interface from array issues	Week 2 Wed
4	Driver calibration check	Output drivers and termination sane before trusting any eye measurement	Week 2 Fri

Nobody in the thread objects to any of this. The scope, the headquarters cadence, the test engineer’s dates and the tester plan are not in dispute.

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Appendix B

B The thread in order, line by line

The timestamps in the forwarded chain are rendered in different clocks, so the hours do not line up. The order below is the reply order, which is unambiguous. Where a name has been replaced inside a quote, the replacement is in brackets [1].

1. The project manager. Link to the status report. Four fields per task: started, finished, days remaining or predicted end, notes. Blue cells to fill. Routine.

2. The program lead. Update the schedule to accelerate blind assembly with aggressive durations. The Taiwan director leads with the foundry, the assembler and the Japan DRIs (directly responsible individuals). The external tester advisor helps with assembler prioritization. The design lead's plan attached.

3. The Taiwan director, first reply. "[The assembly lead] is the key player who works with [the assembler] closely and chairs bi-weekly meeting between [the assembler] and [the company]. I would help him to communicate it with [the assembler] if needed." Translation: the assembly lead owns the assembler relationship. The Taiwan director will support, not lead, that conversation. The program lead's instruction has been quietly narrowed.

4. The Japan assembly lead. "I need wafer information (Parts No, Lot No) to issue PO to [the assembler]." Translation: the purchase order is blocked on data. Nothing else.

5. The Taiwan director, second reply. A screenshot of the foundry's WIP table with the lot ID and wafer numbers circled (two wafers, status HOLD), and: "we will send those 2 [product] wafers to [the assembler]. Pls raise it if any objection by end of today, then I will start shipping process tomorrow." Translation: here is the data the assembly lead asked for; this is a decision by silence with a one-day fuse.

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6. The Japan test director. The message that needs translating. Line by line:

What he wrote	What it means
“we’d like to make a clear the wafer shipment to [the assembler]”	I want to clarify the wafer shipment before it goes.
“we have three wafers with full patter in [the foundry]”	There are three fully patterned wafers at the foundry.
“one of three wafers is a bit issue of characterization, if I’m not wrong”	One of the three is tied up with characterization. The likelier reading is that it is allocated to characterization and not available; the other reading is that characterization found a problem with it. The English does not settle which.
“we focus on other two wafers for CP program debugging”	Japan is counting on the other two for CP (chip probe, the wafer-level test) program debugging. Two readings: either “yes, those are the right two to send,” or “those are the wafers we need at wafer level; if you ship them for assembly they get diced and we lose our CP debug vehicle.” The second reading is a direct conflict with the Taiwan director’s plan.
“two wafer shipment means that we assemble it as DDP package. It takes a long time for the process set up.”	The assembler will read a two-wafer shipment as a dual-die package build. DDP needs a process setup at the assembler and that takes a long time.
“In case of urgency, we should consider an SDP package.”	If speed matters, build single-die packages. This agrees with the design lead, who already said a single-die package is sufficient.
“Of course, we rely on [headquarters]’s decision.”	Japan will not make this call. Headquarters must.
“[The assembly lead] is starting to talk to [the assembler].”	The assembler conversation has started in parallel.

7. Our note to the program lead. The language problem. Teams writing in their second or third language, no native speaker in Japan on the company side, and a thread where the pushback is invisible.

The three ambiguities headquarters should not leave open

Wafer identity. The plan’s row 1 names two sets: “the 3 setup wafers” (two become pipeline cleaners, sacrificial wafers that run through the line first to prove the process) and “2 product wafers” moved from the foundry. The Japan test director names one set: “three wafers with full pattern.” The Taiwan director’s screenshot shows two wafers from one lot. Whether the Japan director’s three are the plan’s three setup wafers, or include the product pair, is not stated anywhere.

CP debug. The Japan director’s “we focus on other two wafers for CP program debugging” is either a confirmation or an objection. Headquarters needs to know which before the wafers are diced.

Package. The plan allows either package. The Japan director says DDP is slow. The Taiwan director’s “2 wafers” framing is being read in Japan as a DDP commitment. The package choice drives the assembly request and the fixture board. It also sets the pin map in the test program skeleton; the plan’s cascade table lists “single die or DDP”. It is the one decision that touches all three workstreams and it has not been made.

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Appendix C

Decisions and a suggested reply

Decision	Who holds it today	Who should	By when
SDP or DDP	nobody	Design lead, program lead on copy	today, before the wafers ship
Which two wafers ship (lot and wafer number)	Taiwan director has proposed; Japan test director has questioned	Taiwan director to confirm; Japan test director to confirm CP debug is unaffected	before the wafers ship
What the PO still needs	Japan assembly lead	Taiwan director to supply	today
Who owns the assembler build end to end	Taiwan director per the program lead; assembly lead per the Taiwan director	name one person in writing	now

Suggested reply for the design lead to send

To the Japan test director, the Taiwan director and the assembly lead — to close this before the wafers move:

1. Package: we build SDP (single die, upper position empty). Do not set up a DDP flow for this build.
2. Wafers: the two wafers in the Taiwan director's table ship to the assembler for blind assembly. Japan, please confirm this does not take away the wafers you need for CP program debug. If it does, say so and we will decide which need comes first.
3. Assembly lead: tell us exactly what you still need for the PO and the Taiwan director will supply it today.

Decision owner for anything on this build is [name]. Reply to this mail, not by silence.

It answers the question the Japan director asked and gives the assembly lead what he needs. It also turns a decision by silence into a decision by reply, the only kind that survives a language gap.

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Sources

References

1 Weekly refresh planning email thread, client program, November 2026. Private correspondence; names, company and product identifiers removed. Held by lateralworks.

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