A lateralworks case study in decision by silence

Every message, translated line by line

November 2026 · lateralworks · Source: a client email thread, names and identifiers removed [1] · Companion to the one-page summary

Messages are in reply order; the clock stamps in the forward are in mixed time zones and are not used. Quotes are verbatim, including the spelling; a replaced name inside a quote is in brackets. Where a line has two possible readings, both are given. Three terms, defined once: DDP is a dual-die package, two die stacked; SDP is a single-die package; CP is chip probe, the wafer-level test.

#	From	What they wrote (verbatim)	What it means	Why it matters
1. The project manager: sets up the weekly refresh				
1	**Project manager**	*“Below is the link to the status report… Blue cells need to be filled in! If you see any red cells, it’s an invalid update so please fix.”*	Fill in your task status before the meeting. Red means your entry is not valid.	Routine. The refresh runs on this sheet; nothing in the thread changes it.
2. The program lead (headquarters): sets direction				
2	**Program lead**	*“Let’s ensure that we update the schedule to accelerate blind assembly builds using aggressive durations. See below from [the design lead]. We need to turn on the afterburners!”*	The design lead’s plan is the plan. Put it in the schedule with the shortest durations anyone will sign up to.	Headquarters has adopted the plan. Everything after this is execution, not debate.
3	**Program lead**	*“[The Taiwan director] can take the lead working with [the foundry], [the assembler] and our Japan Team DRI’s (directly responsible individuals)… [The external advisor] can help on [the assembler] prioritization if needed.”*	The Taiwan director owns the build end to end: the foundry, the assembler and the Japan owners. The external advisor is the escalation path at the assembler.	This is the only place a single owner is named. The Taiwan director narrows it one message later.
3. The design lead (headquarters): the plan, sent on by the program lead				
4	**Design lead**	*“Recent findings from Silicon Validation make it critically urgent to check whether the [memory] interface works at its target frequencies, up to [full speed].”*	Validation found something that puts the interface speed in doubt. The fast way to know is to package die now, before wafer test has proven them, and test the interface.	The reason for the urgency. Every date in the plan hangs on this.

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5	**Design lead**	*“We have identified 4 test items… that can be run early to tell us whether the interface of the chip works at frequency. No memory array access is required at this stage. It is a stretched goal to intercept further silicon with metal fixes.”*	Four interface-only tests, no memory array needed. If they finish in time, fixes can go into the next silicon in the metal layers.	Scope is deliberately small. Nobody should add tests to this build.
6	**Design lead**	*“Package: a single-die package (upper die position left empty) is sufficient for these tests. If the standard DDP route is faster at [the assembler], please go ahead with the default DDP — the test program covers both.”*	One die per package is enough. Build dual-die only if the assembler is quicker that way. The test program works either way.	A conditional decision. Japan later says DDP is slower, which by this rule makes it SDP. Nobody has written that down.
7	**Design lead**	*“Assembly hardware to be requested immediately; [the Taiwan director] to provide daily support. The setup wafers go first as a mechanical trial (to take less than one week), then the 2 [product] wafers follow straight away.”*	Order the assembly hardware now. Run the setup wafers through first to prove the process in under a week, then the two real wafers.	Two sets of wafers: setup wafers, then product wafers. The Japan test director later refers to only one set of three.
4. The Taiwan director: first reply				
8	**Taiwan director**	*“In general, [the assembly lead] is the key player who works with [the assembler] closely and chairs bi-weekly meeting between [the assembler] and [the company]. I would help him to communicate it with [the assembler] if needed.”*	The assembly lead owns the assembler, not me. I will support him.	The program lead’s single owner is now two people. The assembler build has a lead and a helper, and nobody has said which is which in writing.
9	**Taiwan director**	*“Pls raise it if needs any helps from myself.”*	Assembly lead, ask me if you need anything.	Polite; also a signal that the Taiwan director is waiting to be asked, not driving.
5. The Japan assembly lead				
10	**Assembly lead**	*“I need wafer information(Parts No, Lot No) to issue PO to [the assembler].”*	I cannot raise the purchase order until someone gives me the part number and lot number.	The PO is blocked on data, not on a decision. Easy to clear; nobody had cleared it.

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6. The Taiwan director: second reply				
11	**Taiwan director**	*“Pls see below, we will send those 2 [product] wafers to [the assembler].” (with a foundry WIP screenshot: two wafers, one lot, status HOLD)*	Here are the lot and wafer numbers the assembly lead asked for. These two go to the assembler.	Answers the assembly lead. Also quietly decides which wafers ship.
12	**Taiwan director**	*“Pls raise it if any objection by end of today, then I will start shipping process tomorrow.”*	Silence by the end of my day means I ship tomorrow.	A decision by silence with a one-day fuse, across three time zones and three languages. The next message is the silence being broken, and it does not look like it.
7. The Japan test and assembly director: the message that needs translating				
13	**Japan test director**	*“However, we’d like to make a clear the wafer shipment to [the assembler].”*	I want to clarify the wafer shipment before it goes.	“However” is the objection. It is the only word of it.
14	**Japan test director**	*“Our understanding is that we have three wafers with full patter in [the foundry].”*	There are three fully patterned wafers at the foundry.	One set of three. The plan has “3 setup wafers” and “2 [product] wafers”. Whether these three are the setup wafers, or include the product pair, is not stated.
15	**Japan test director**	*“And, one of three wafers is a bit issue of characterization, if I’m not wrong.”*	One of the three is tied up with characterization. The likelier reading: it is allocated to characterization and not available. The other: characterization found a problem with it.	The English does not settle which. Either way, only two wafers are free.
16	**Japan test director**	*“So, we focus on other two wafers for CP program debugging.”*	Japan is counting on the other two for CP program debug (CP is chip probe, the wafer-level test). Two readings: “yes, those are the right two to send”, or “we need those two at wafer level; ship them for assembly and they get diced and we lose our CP debug vehicle”.	The line with real consequences. The second reading is a direct conflict with the Taiwan director’s plan and nobody at headquarters will see it as one.

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17	**Japan test director**	*“On the other hand, two wafer shipment means that we assemble it as DDP package. It takes a long time for the process set up.”*	The assembler will read a two-wafer shipment as a dual-die package build. DDP needs a process setup at the assembler, and that setup is slow.	Cuts against the whole point of the exercise. The Taiwan director’s “2 wafers” is being read in Japan as a DDP commitment.
18	**Japan test director**	*“In case of urgency, we should consider an SDP package.”*	If speed matters, build single-die packages.	Agrees with the design lead, who already said a single-die package is sufficient. By the design lead’s own rule this closes the question: SDP.
19	**Japan test director**	*“Of course, we rely on [headquarters]’s decision.”*	Japan will not make this call. Headquarters must.	The decision now has no owner. Taiwan is waiting for silence; Japan is waiting for headquarters; headquarters thinks Taiwan has it.
20	**Japan test director**	*“On the other hand, [the assembly lead] is starting to talk to [the assembler].”*	The assembler conversation has started in parallel.	The assembler may hear “two wafers” before anyone has said “SDP”.
8. Our note to the program lead: the forward				
21	**lateralworks**	*“So much of this is a language problem. A year ago you needed a [native] speaker on the team, located in Japan… You have teams speaking their second/third language, what could go wrong.”*	The plan is fine. The reading of it is not. The pushback above is invisible to anyone reading in a hurry.	The fix is a person, not a process: a native speaker in Japan on the company side, and a rule that decisions are made by reply, never by silence.

What the table adds up to: the plan is agreed by everyone. Three things are not: whether the two wafers the Taiwan director named are the two Japan needs for CP debug, whether the package is SDP or DDP, and who owns that decision. The design lead’s own rule already answers the second; the first and third need one reply from headquarters today, by email rather than by silence.

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Sources

References

1 Weekly refresh planning email thread, client program, November 2026. Private correspondence; names, company and product identifiers removed. Held by lateralworks.

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